

**BEST AVAILABLE COPY**REMARKSApplicant's Statement of Substance of Interview

Applicants wish to express appreciation to Examiners Wenpeng Chen and Manav Seth for the courtesy of a personal interview which was granted to Applicants' representative Michael Faibisch (Reg. No. 48,427) at the USPTO on June 28, 2005. The Examiner's statement of the substance of the interview is set forth in the Interview Summary, numbered Paper No. 20060628. During the interview, claims 1 and 12 were discussed vis-à-vis the Valesio, Yamamoto et al. and Aloni references. Applicants' representative proposed amending the claims to point out that the inspection system and method employs boundaries in an electrical circuit to detect element matching defects and boundary defects. Applicant would file amendment. Further search and consideration would be required. No agreement was reached.

Priority Document

As noted in the interview summary, the Examiner pointed out that the priority document was not supplied by the Applicant. Applicant respectfully submits that a certified copy of the priority document was filed in the parent application, Serial Number 09/633,756, on December 5, 2005.

General Remarks

Claims 1 – 15, 18, 20 – 24, and 27 are pending in the application. Claims 1, 3, 4, 5, 7 – 12, 20 and 21 include amendments as seen above and discussed below.

Applicant has carefully studied the outstanding Office Action in the present application. The present amendment is intended to be fully responsive to all points of rejection raised by the Examiner in the Office Action mailed March 1, 2006, and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of all claims under consideration is respectfully requested.

Prior Art Rejections

Claims 1 – 8, 12 – 15 and 21 – 24 stand rejected under 35 USC §103(a) as being unpatentable over Valesio et al. (FR 2 687 091), Yamamoto et al. (JP Patent Publication No. 08-

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327560) and Aloni et al. (US 5,619,429). Claims 9, 10, 11, 18, 20 and 27 stand rejected under 35 USC §103(a) as being unpatentable over Valesio et al. (FR 2 687 091), Yamamoto et al. (JP Patent Publication No. 08-327560), Aloni et al. (US 5,619,429) and Bachelder (US 5,974,169).

Valesio et al. (FR 2,687,091) describes a process for computer assisted inspection of cutouts made in a tape by a cutout machine. The inspection method includes extracting contours (boundaries) defining the cutouts and making a polygonal approximation of the cutout. Segments of the polygonal approximation are vectorized, and the series of angles between successive segments are compared with corresponding angles in a theoretical cutout to detect defective cutouts. Yamamoto et al. (JP Patent Publication No. 08-327560), as best understood, describes a device and method for rapidly inspecting a shape by converting plural points on a contour of an image to a chain code and determining whether the length of the chain code is within an allowable error by comparison to a reference. Aloni et al. (US 5,619,429) describes apparatus and a method for inspection of a patterned object (an electrical circuit) by comparison of the object to a reference. The apparatus and method include hardware defect detection and software postprocessing. Bachelder (US 5,974,169) describes machine vision methods for determining characteristics of an object using boundary points and bounding regions.

Independent claim 1 has been amended and now includes, *inter alia*, the following distinguishing recitation:

an element matching defect identifier operative to receive said representation of boundaries of elements and a reference representation including reference boundaries for said electrical circuit and to compare boundaries in said representation of boundaries to said reference boundaries to identify element matching defects, said element matching defects including at least one of: elements in said reference representation but missing from said representation of boundaries, excess elements in said representation of boundaries that are missing from said reference representation, and elements in said representation of boundaries defining a different type of element than a corresponding element in said reference representation; and

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a boundary defect identifier operative to receive said boundaries of elements in said electrical circuit under inspection and to compare a plurality of coordinates along at least a portion of some boundaries with reference to a corresponding region of acceptable coordinates for said portion of some boundaries to detect boundary defects.

Independent claim 12 has been amended and now includes, *inter alia*, the following distinguishing recitation:

detecting element matching defects by comparing said boundaries in said representation of boundaries to reference boundaries in a reference representation of boundaries for said electrical circuit, said element matching defects including at least one of: elements in said reference representation but missing from said representation of boundaries, excess elements in said representation of boundaries that are missing from said reference representation, and elements in said representation of boundaries defining a different type of element than a corresponding element in said reference representation; and

and comparing a plurality of coordinates along at least a portion of said boundaries in said representation of boundaries of elements with reference to a corresponding region of acceptable coordinates for said portion of said boundaries to detect boundary defects in said electrical circuit.

Independent claim 21 has been amended and now includes, *inter alia*, the following distinguishing recitation:

detecting element matching defects by comparing said boundaries in said representation of boundaries to reference boundaries in a reference representation of boundaries for said electrical circuit, said element matching defects including at least one of: elements in said reference representation but missing from said

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representation of boundaries, excess elements in said representation of boundaries that are missing from said reference representation, and elements in said representation of boundaries defining a different type of element than a corresponding element in said reference representation; and

comparing a plurality of coordinates along at least a portion of said boundaries in said representation of boundaries of elements with reference to a corresponding region of acceptable coordinates for said portion of said boundaries to detect boundary defects in said electrical circuit portion.

Support for the amendment of claims 1, 12 and 21 can be found, *inter alia*, in the written specification at paragraphs 326, 438 – 441, 471, 545, 546, 650 – 678, and in Figures 24 – 32B of the drawings.

As pointed out by the Applicants' representative with reference to claims 1 and 12 in the interview held on June 28, 2006, nothing in any of the prior art of record shows or describes, alone or in combination, employing boundaries generated from an image of an electrical circuit to detect element matching defects and to detect boundary defects.

With reference to Valesio et al., it is noted that the defects detected there (which are detected by means of comparing angles between successive vectorized segments) are whether an inspected polygon is properly shaped. With reference to Bachelder, it is noted that the boundary points in an image are matched with edges in a real world object. Neither Valesio et al. nor Bachelder, however, shows or describes, *inter alia*, detecting element matching defects including at least one of: (i) elements that are in a reference representation but missing from the representation of boundaries of an electrical circuit being inspected, (ii) excess elements in the representation of boundaries of an electrical circuit being inspected that are missing from the reference representation of boundaries, and (iii) elements in the representation of boundaries of an electrical circuit being inspected that define a different type of element than a corresponding element in the reference representation of boundaries. This feature is likewise not shown or described in Yamamoto et al.

Furthermore it is respectfully submitted that the Yamamoto methodology of converting a boundary to a chain code, and then determining whether the length of the chain code is outside

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an allowable error for the chain code length, in order to determine whether a boundary is possibly defective, is fundamentally different than comparing a plurality of coordinates along at least a portion of a boundary in the representation of boundaries of elements with reference to a corresponding region of acceptable coordinates for the portion of said boundaries to detect boundary defects. No reasonable person skilled in the art would equate determining whether the length of a chain code is outside an acceptable error with comparing coordinates of an inspected boundary to a region of acceptable coordinates for the boundary, as required by each of claims 1, 12 and 21. Likewise, neither the Valesio et al. nor Bachelder references compares a plurality of coordinates along at least a portion of a boundary in the representation of boundaries of elements with reference to a corresponding region of acceptable coordinates for the portion of said boundaries to detect boundary defects as required by each of claims 1, 12 and 21.

With reference to Aloni et al., it is noted that no use is made of boundaries in the inspection of electrical circuits.

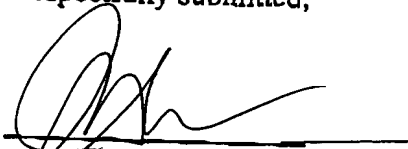
Applicants thus respectfully submit that the combined teachings of the prior art documents, even if taken together for what they would have meant as a whole to an artisan of ordinary skill, fail to meet the above-identified requirements of the claims as now amended. In view of the foregoing, Applicants respectfully request that the Examiner withdraw the rejection of independent claims 1, 12 and 21, and all of their dependent claims 2-11, 13-15, 18, 20, 22-24 and 27, under 35 USC §103(a).

**Conclusion and Request for Interview**

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. \_\_\_\_\_. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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